RSTGEN IP SPEC

Table of Contents

[Introduction 2](#_Toc120195827)

[Feature 2](#_Toc120195828)

[Functional Details 2](#_Toc120195829)

[Block Diagram 2](#_Toc120195830)

[Module input/output list 2](#_Toc120195831)

[Clock Definition 3](#_Toc120195832)

[RSTGEN function description 4](#_Toc120195833)

## Introduction

The RSTGEN module is used to generate reset signals for other digital modules.

## Feature

Output reset signals include hardware reset, hardware and software reset. Both reset signals are scan-muxed by SCAN\_MODE.

## Functional Details

### Block Diagram

The following diagram shows the main inputs and outputs of RSTGEN.



Figure1 RSTGEN diagram

### Module input/output list

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Dir | Width | Discirption | duration |
| resetb\_CLK\_256K | O | 1 | Scan-muxed resetb for CLK\_256K domain | level |
| resetb\_CLK\_OUT | O | 1 | Scan\_muxed resetb for CLK\_OUT domain | level |
| resetb\_SR\_CLK\_OUT | O | 1 | Scan\_muxed resetb and soft resetb for CLK\_OUT domain | level |
| resetb\_SR\_CLK\_SLOW | O | 1 | Scan\_muxed resetb and soft resetb for CLK\_SLOW domain | level |
| resetb\_CLK | O | 1 | Scan\_muxed resetb for CLK\_32M domain | level |
| resetb\_SR\_CLK\_I2C | O | 1 | Scan\_muxed resetb and soft resetb for CLK\_I2C domain | level |
| rstb\_32M\_OK | O | 1 |  |  |
| rstb\_32M\_ok\_and\_sr | O | 1 | CLK\_32M\_OK high and SOFT\_RSTB high | level(CLK\_32M domain) |
| SOFT\_RSTB\_32M | O | 1 | SOFT\_RSTB\_REG synchronized to CLK\_32M domain | level |
| resetb\_32M\_no\_sc | O | 1 | Resetb for CLK\_32M domain(no scan-mux) | level |
| SCAN\_MODE | I | 1 | DFT scan mode |  |
| SCAN\_RSTB | I | 1 | DFT scan resetb |  |
| CLK\_32M | I | 1 | Main clock from analog |  |
| CLK\_256K\_SC | I | 1 | Scan\_muxed CLK\_256K |  |
| DRSTB | I | 1 | Async digital reset |  |
| CLK\_OUT\_SC | I | 1 | Scan\_muxed CLK\_OUT |  |
| CLK\_SLOW\_SC | I | 1 | Scan\_muxed CLK\_SLOW |  |
| SOFT\_RSTB\_REG | I | 1 | SOFT\_RSTB register bit |  |
| SOFT\_RSTB | I | 1 | SOFT\_RSTB in CLK\_SLOW domain |  |
| CLK\_32M\_ORG\_SC | I | 1 | Scan\_muxed original CLK\_32M |  |
| CLK\_32M\_SC | I | 1 | Scan\_muxed CLK\_32M |  |
| I2C\_MAS\_EN | I | 1 | I2C master enable register bit |  |
| CLK\_32M\_OK | I | 1 | CLK\_32M status from analog | Level(async) |

### Clock Definition

The following table describes clocks defined in Figure 1 block diagram and other sections of this document.

|  |  |
| --- | --- |
| Clock Name | Definition |
| resetb\_CLK\_256K | CLK\_256 domain |
| resetb\_CLK\_OUT | CLK\_OUT domain |
| resetb\_SR\_CLK\_OUT | CLK\_OUT domain |
| resetb\_SR\_CLK\_SLOW | CLK\_SLOW domain |
| resetb\_CLK | CLK\_32M domain |
| resetb\_SR\_CLK\_I2C | CLK\_32M domain |
| rstb\_32M\_ok\_and\_sr | CLK\_32M domain |
| SOFT\_RSTB\_32M | CLK\_32M domain |
| resetb\_32M\_no\_sc | CLK\_32M domain |

Table1 clock definitions

### RSTGEN function description

For different sub-modules, reset signals are generated for corresponding clock domain.

Hr\_b change to 0 synchronously when DRSTB low and released synchronously when DRSTB high. Hr\_b is a group of reset signals, include resetb\_CLK, resetb\_CLK\_OUT and resetb\_CLK\_SLOW. (HWR001\_RSTGEN)

Hr\_sr\_b change to 0 synchronously when DRSTB low, change to 0 synchronously when SOFT\_RSTB\_REG low, released synchronously when DRSTB and SOFT\_RSTB\_REG high. Hr\_sr\_b is a group of reset signals, include resetb\_SR\_CLK\_OUT, resetb\_SR\_CLK\_SLOW and resetb\_SR\_CLK\_I2C. (HWR002\_RSTGEN, HWR003\_RSTGEN)

All signals in hr\_b and hr\_sr\_b are scan-muxed. When SCAN\_MODE high, they all connected to SCAN\_RSTB. (HWR004\_RSTGEN)